**Amendments to the Drawings:**

The attached drawing sheet includes new Figs. 1-5, which figures are believed to have improved reproducibility.

## REMARKS

In the first Office Action dated December 4, 2010, the drawings were objected to as being informal because of "poor reproducibility." Attached to this paper are new Figs. 1-5, which are believed to have improved reproducibility. Accordingly, withdrawal of the drawing objection is respectfully requested.

Further in the first Office Action, claims 6, 20, 24, 26, 28 and 29 were objected to as being informal for improperly using terms such as "specific," "specifically," and "specially." With this paper, these terms have been removed from claims 6, 20, and 29 and claims 24, 26 and 28 have been canceled. Hence, withdrawal of the claim objections is respectfully requested.

Claims 1-22 and 24-29 were rejected under 35 U.S.C. § 112, ¶ 2 as being indefinite. With this amendment, claims 1, 6, 11, 12, 13, 20 and 29 have been amended so as to overcome the objections made regarding these claims. Further, claims 24, 26 and 28 have been canceled. Accordingly, withdrawal of the § 112 rejection is respectfully requested.

Still further in the Office Action, claims 1, 20, 24 and 26 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,583,029 to Abe et al.

Claim 1 has been amended to include a limitation very similar to one previously found in dependent claim 6, namely, "a front side facet having a length, measured in a direction of the surface, of less than 75 μm in each of the two semiconductor wafers." Since claim 6 was not rejected based on prior art grounds, it is respectfully submitted that amended claim 1 and its dependent claims are novel and nonobvious. It is additionally believed that claim 1 and its respective dependent claims define patentably over the applied prior art for the following reasons. It is also submitted that independent claim 20 and its respective dependent claims define patentable subject matter for the following reasons.

The '029 patent discloses a method for manufacturing a mirror polished wafer with little polishing sag (peripheral sag). The '029 patent also discloses a method for manufacturing a bonded SOI wafer comprising a bond wafer and a base wafer and wherein a polishing sag portion is removed, i.e., "the unbonded region between the bond wafer and the base wafer," see column 7, lines 6-10. The '029 patent teaches preparing

one or more silicon wafers having chamfered portions, wherein the chamfering width of a front surface side of the silicon wafer after lapping and etching is X1 and a chamfering width of the back surface side thereof after lapping and etching is X2, such that X1<X2, see column 5. The front surface of the silicon wafer is mirror polished, and the front surface side thereof is chamfered again so that the chamfering width thereof is X3 (X3>X1). It is submitted that the main objective of Abe et al. is to overcome a problem of polishing sag, and, for achieving this objective, several polishing and chamfering steps are performed on the front surface side of at least one wafer, which may be bonded to a second wafer. The objective of reducing a non-usable edge region of a bonded wafer is not addressed by Abe et al. Example dimensions of a chamfer are given by Abe et al. as 300+/-200 μm, see col. 4, lines 19-20, 300 μm, see col. 13, line 27, and as a larger value 350 μm prior to a lapping process, see col. 12, line 52. The overall function of Abe is discussed in col. 4, lines 11-29:

> The present inventors have focused on the chamfering shape before mirror polishing in order to reduce polishing sag of a mirror polished wafer. In the chamfering width of the chamfered portions of a mirror polished wafer manufactured by a typical manufacturing process, as shown in FIG. 4, the size ratio of a chamfering width X1 of the wafer front surface side to a chamfering width X2 of the wafer back surface side is often X1=X2 (for example, 300+/-200μm). Chamfering is performed at least before mirror polishing the front surface. In some applications, X1 and X2 maybe set to different values. Also in this case, chamfering is typically performed before mirror polishing the front surface. In the name of mirror chamfering, the chamfered portion may be mirror polished after mirror polishing the front surface of the wafer. This is performed to chiefly mirror polish the chamfered portion for preventing particles from being generated, but does not vary the chamfering shape in the process.

In contrast, the present invention is directed to reducing a non-usable edge region of a bonded wafer in order to obtain an edge region having as low a number of defects as possible and to obtain a usable wafer surface as large as possible after grinding.

Claim 1, as amended, now recites:

providing a periphery or edge geometry including a front side facet having a length, measured in a direction of the surface, of less than 75 µm in each of the two semiconductor wafers at the surfaces to be bonded;

bonding the two semiconductor wafers at the surfaces to be bonded;

thinning one of the two semiconductor wafers to produce a thinned layer bonded on the other one of the two wafers.

Nowhere does Abe et al. disclose the above noted steps. Nor do they disclose the dimensions of the front side facet in each wafer as now recited in claim 1.

Claim 20, as amended, now recites:

An assembly as a composite of two semiconductor wafers connected by a semiconductor bonding process, wherein the bonded semiconductor wafers are provided at the bonded surfaces with an edge geometry having a front side facet less than 75µm for a wafer diameter ranging from 100m to 300mm so as to obtain an edge region after thinning, as one of separation or splitting off of one of the wafers.

Nowhere does Abe et al. disclose the above structural elements. Nor do they disclose the dimensions of the front side facet in each wafer as recited in claim 20.

In view of the above summary of Abe et al., it is apparent that Abe et al. teach a completely different range of chamfer widths and, therefore, do not teach to one skilled in the art any reduction in the dimension of a chamfer.

Furthermore, Abe et al. achieve a well-defined edge of a donator wafer after thinning only by an additional edge forming step which becomes necessary because of the large chamfer dimension of 300 µm. In the present invention, an additional processing step for achieving a well defined edge of the donator wafer may not be necessary because the short facets of less than 75 µm have the effect that a substantially rectangular edge is produced whereby the donator wafer does not suffer break-outs upon thinning thereof.

In view of the above, it is submitted that independent claims 1 and 20 and their respective dependent claims define patentable invention over Abe et al.

## CONCLUSION

For all of the above reasons, the applicants respectfully submit that the above claims recite allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

STEVENS & SHOWALTER, L.L.P.

By /Robert L. Showalter/

Robert L. Showalter
Registration No. 33,579

7019 Corporate Way
Dayton, OH 45459-4238
Telephone: 937-438-6848
Fax: 937-438-2124
Email: rshowalter@sspatlaw.com

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